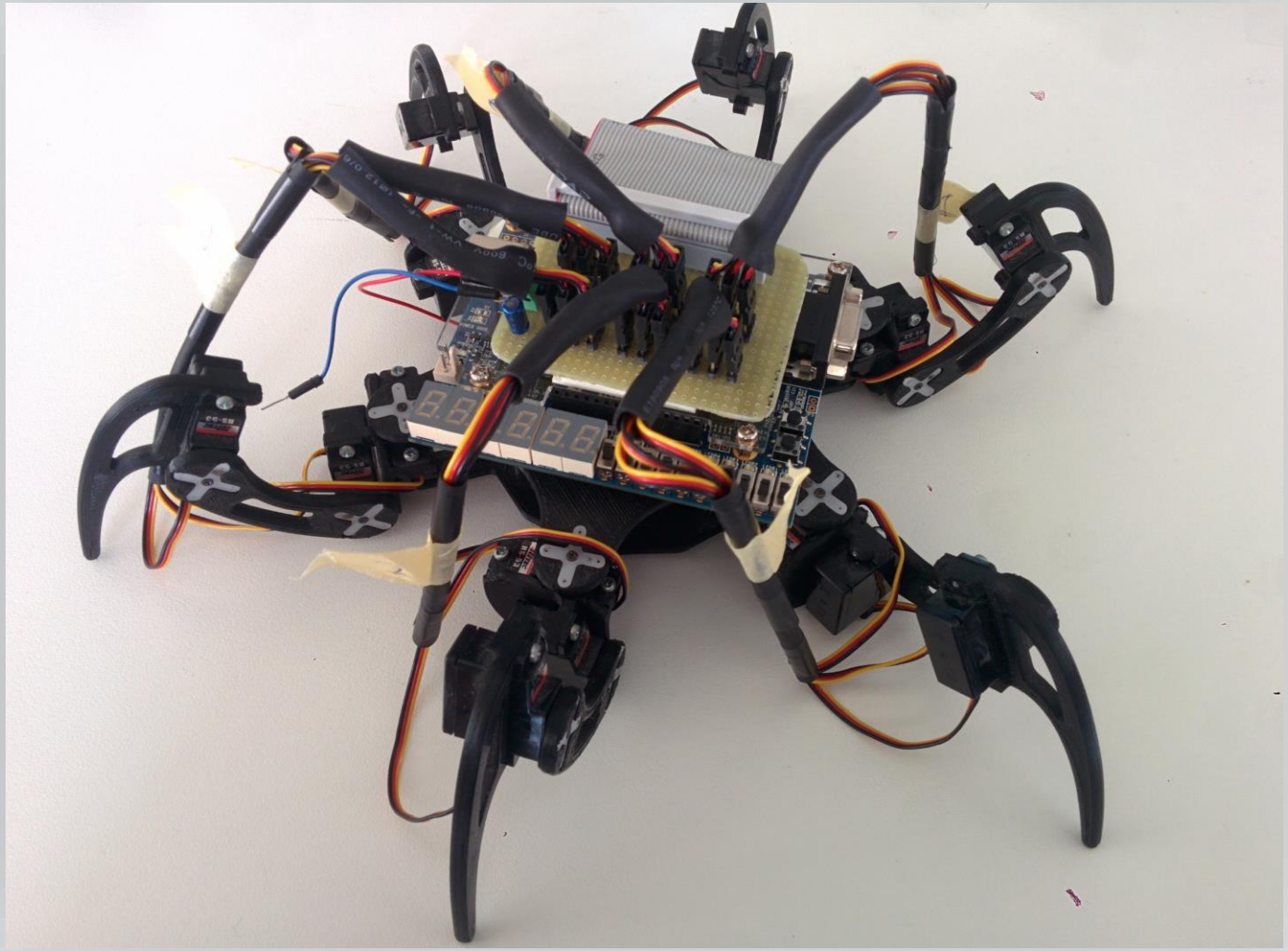
EMBEDDED SYSTEM FOR HEXAPOD CONTROL



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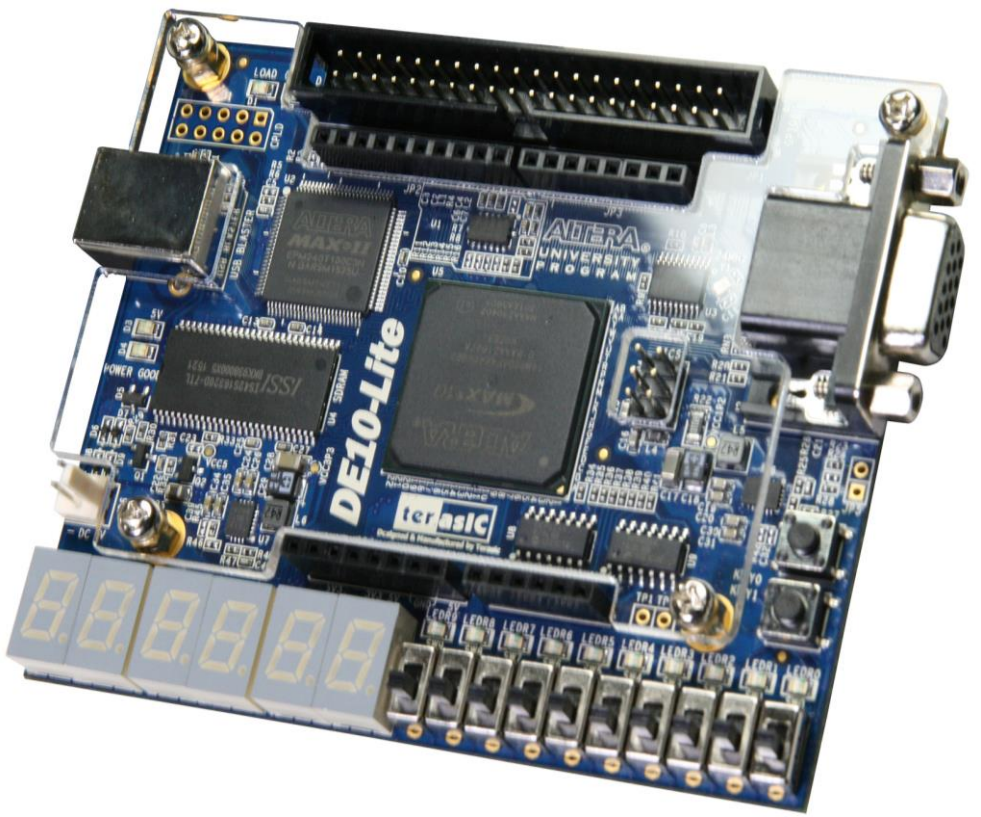
OUR GOALS

Design and implementation of an Embedded Computer ad hoc for Hexapod control

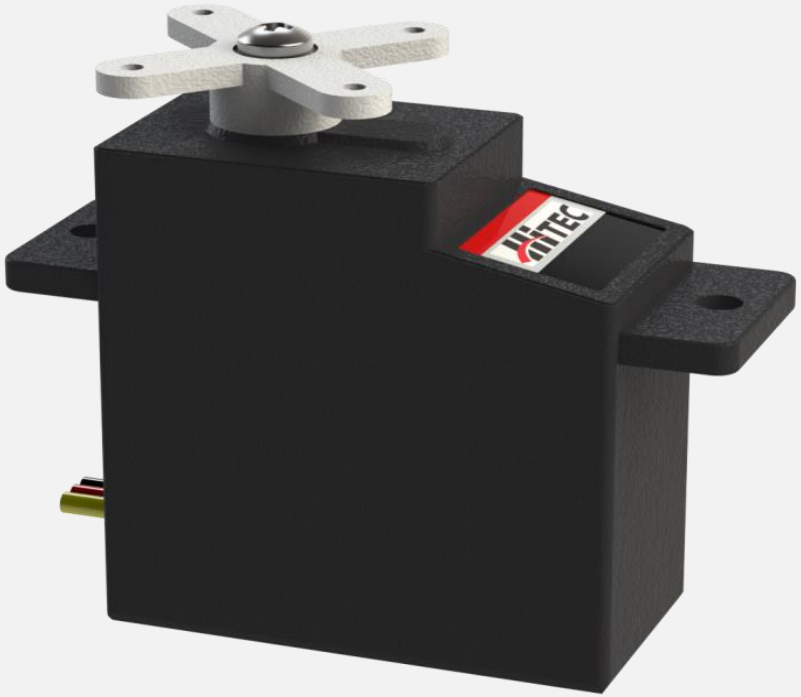
- Use of NiosII/e processor based on Altera FPGA
- Synthesis and fitting of a MotorDriver_V2 component for Micro Servo control
- Code porting from Microchip PIC18 architecture to NiosII architecture

COMPONENTS: TERASIC DE10-LITE



- MAX 10 FPGA
  - MAX 10 10M50DAF484C7G FPGA Device
  - 5,888 Kbits user Flash memory
  - 1,638 Kbits M9K memory (on-chip memory)
- 2x20 GPIO Header
- 10 LEDs
- 2 Push Buttons with Debounced
- Six 7-Segments

COMPONENTS: MICRO SERVO HITEC HS-53



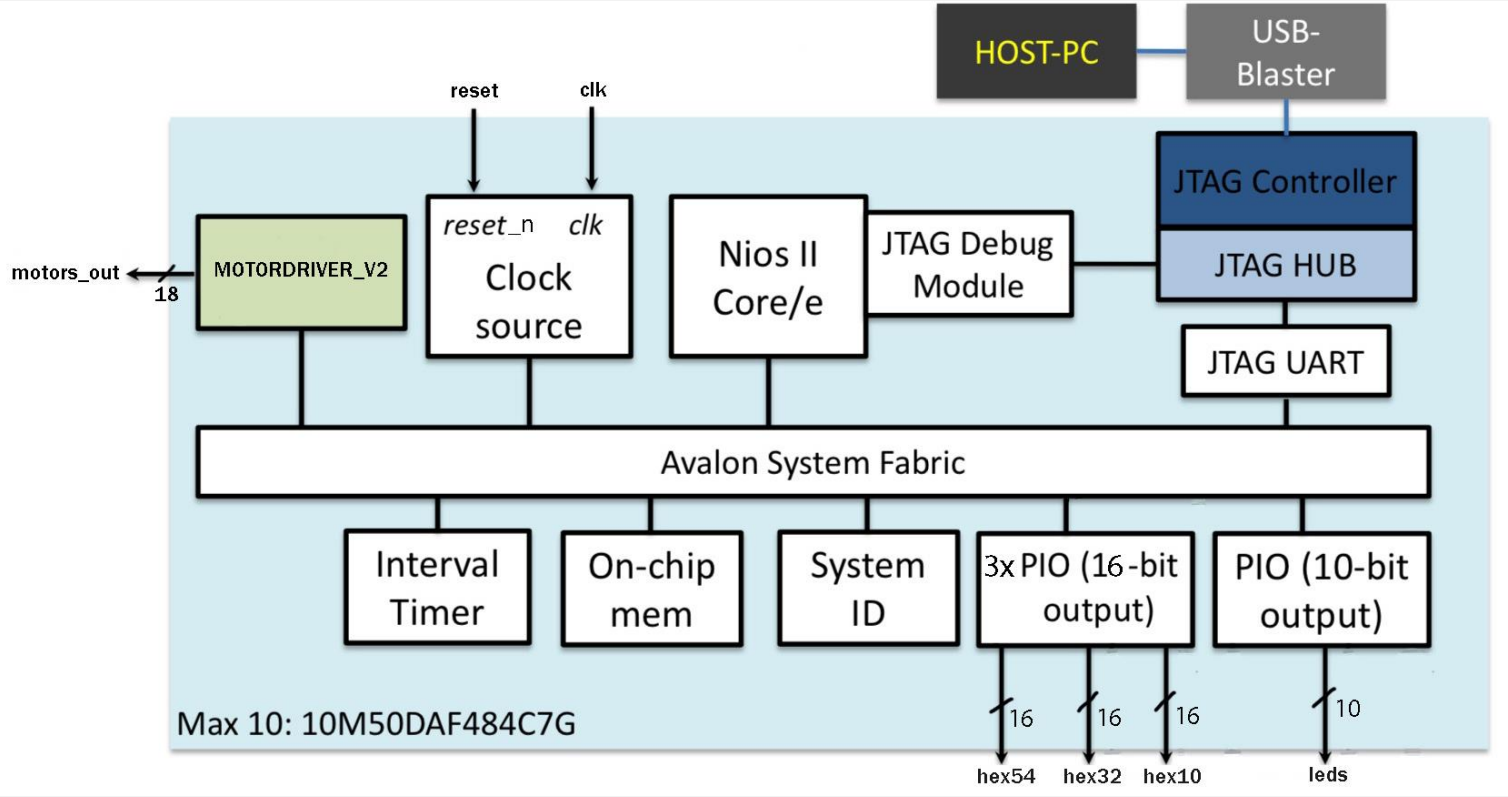
- Supply voltage: 6V
- Dimensions: 22.8 x 11.6 x 22.6 mm
- Weight: 8gr

COMPONENTS: AUGUSTO HEXAPOD

HEXAPOD COMPUTER

Designed on Quartus Prime 16.1 tool: Qsys

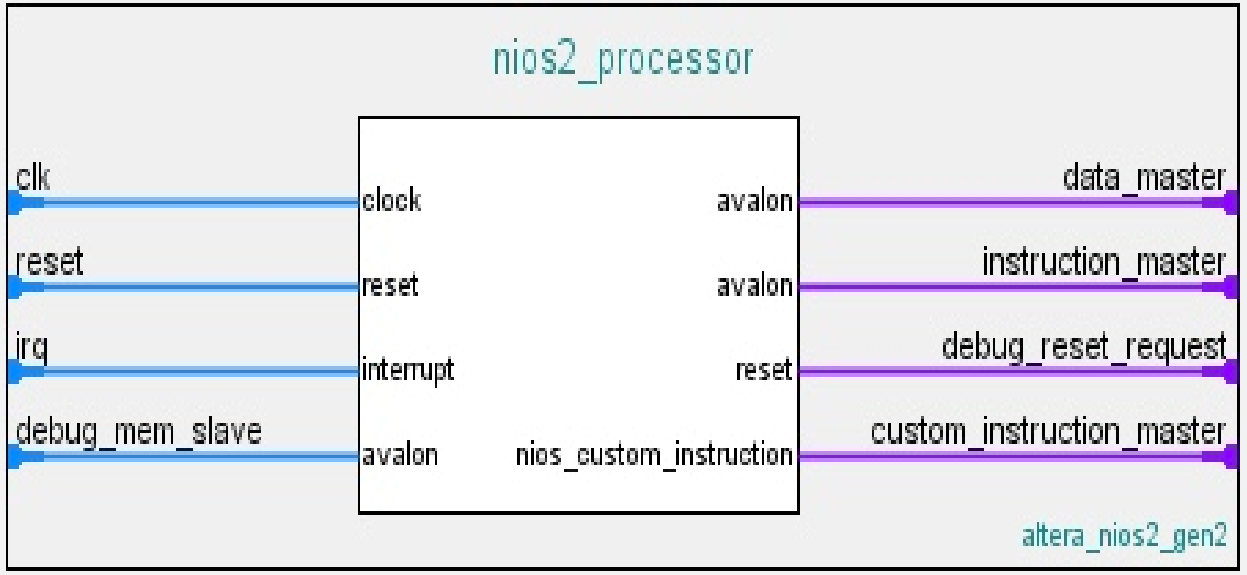
- Clock source
- NiosII Processor
- On-Chip Memory
- System ID Peripheral
- JTAG UART
- Interval Timer
- 4 x PIO (Parallel I/O)
- MotorDriver_V2



MAIN COMPUTER'S COMPONENTS: NIOSII PROCESSOR

NiosII Processor main features:

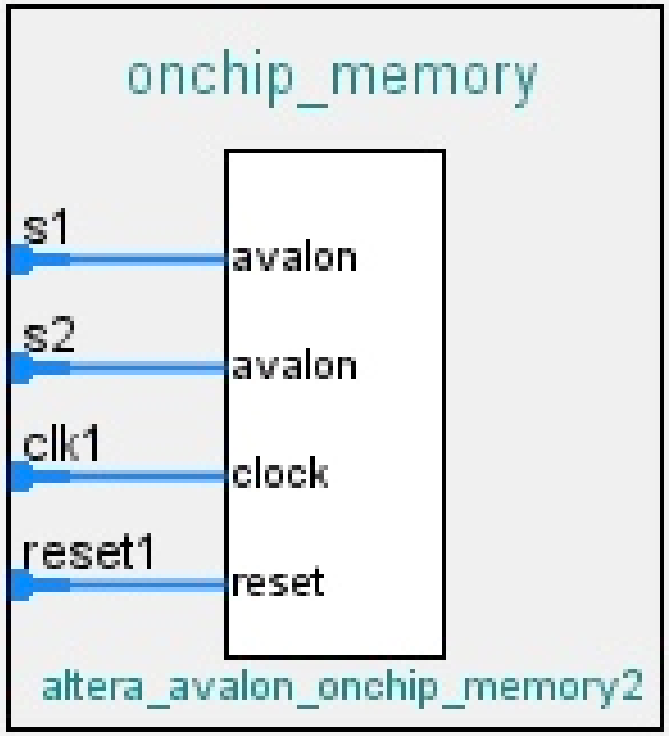
- Economy version
- Complete processors in fewer than 700 LEs
- Resource-optimized 32bit RISC architecture
- JTAG debug module



MAIN COMPUTER'S COMPONENTS: ON-CHIP MEMORY

On-Chip memory main features:

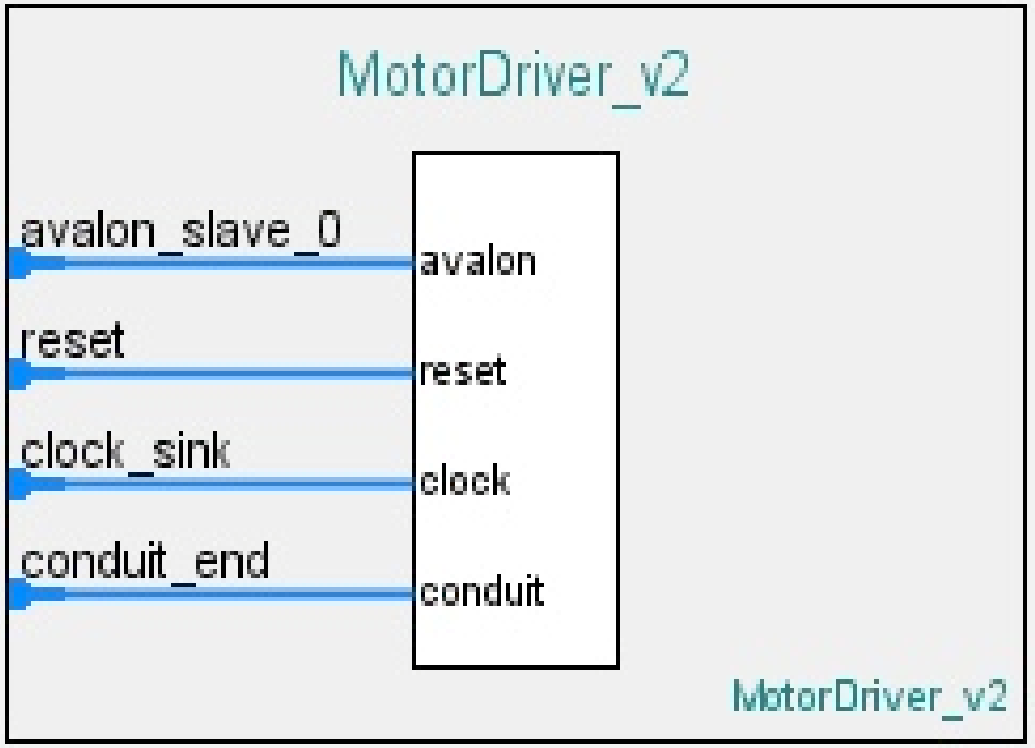
- Memory type: RAM
- Dual-port access (Harvard Architecture)
- Bus width: 32 bits
- Total memory size: 174080 Bytes
- Non default memory initilization



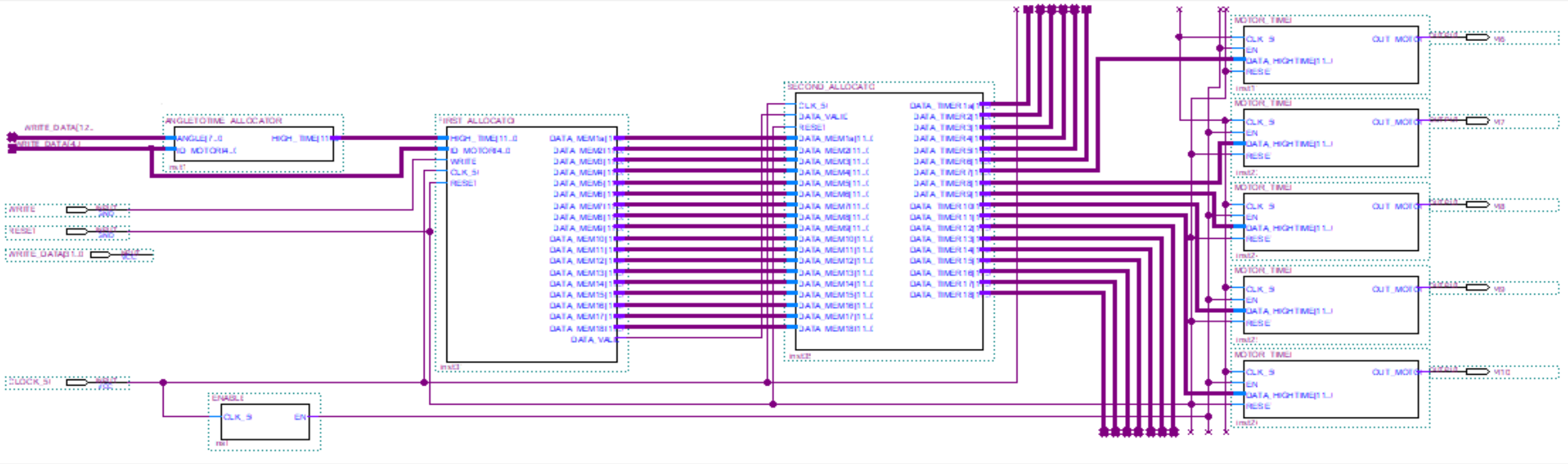
MAIN COMPUTER'S COMPONENTS: MOTORDRIVER_V2

MotorDriver_V2 main features:

- Avalon MM Slave interface to NiosII processor
- Write only "registers" with WRITE and WRITE_DATA[31:0] signals
- Avalon Clock interface
- Avalon Reset interface
- 18 x Avalon Conduit interfaces from MotorDriver_V2 to servo motors



MOTORDRIVER_V2: ARCHITECTURE



MOTORDRIVER_V2: COMPONENTS

- ANGLETOTIME_ALLOCATOR_V2

  Conversion from angle to Ton of PWM signal

- FIRST_ALLOCATOR

  18 registers sequential memory buffer

- SECOND_ALLOCATOR

  18 registers parallel memory buffer

- MOTOR_TIMER

  PWM signal generator

- ENABLE

  1MHz enable for MOTOR_TIMER

MOTORDRIVER_V2: SYNTHESIS, FITTING AND SIMULATION

Analysis and Synthesis report:

- Total logic elements: 1018
- Total Registers: 689

Place and Route report:

- Total logic elements: 801
- Total Registers: 689

Slow Timing Analysis:

- Fmax: 57.57 MHz
- Slack on Tsetup: 2.631 ns
- Slack on Thold: 0.412 ns

HEXAPOD CONTROL CODE

- Code porting from 2 x Microchip PIC18 (8 bits microcontroller) architecture to NiosII architecture (32 bit processor)
- Use of alt_types library for integer types in NiosII architecture
- Use of header files for better organization of code

HEXAPOD EXHIBITION

Let's see the Hexapod's exhibition by NiosII terminal…